

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Simon C. Steely JR

Examiner: John A. Lane

P.003/004

Serial No.:

09/843,228

Group Art Unit: 2188

Filed:

April 26, 2001

Docket No.: 200308272-1

Title:

Low Latency Inter-Reference Ordering in a Multiple Processor System

Employing a Multiple-Level Inter-Node Switch

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop: Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Please enter the following Response to Examiner's Reasons for Allowance. Remarks begin on page 2.

AUTHORIZATION TO DEBIT ACCOUNT

It is believed that no extensions of time or fees for net addition of claims are required, beyond those, which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Date: January 20, 2005



REMARKS

In the Examiner's reasons for allowance, the Examiner states (text omitted):

The art of record does not teach the claimed multiple-processor system comprising "a plurality of nodes ... and follows the same ordering rule simultaneously."

Applicant agrees that the art of record does not teach or suggest the recited limitations. Applicant submits that the present claims are allowable for at least the reason that the art of record does not teach or suggest all of the limitations of the claims as recited in the claims themselves. Each claim is allowable in light of the complete language of the claim, as well as equivalents. The Applicant therefore respectfully asserts that the scope of each claim as allowed is to be determined from the actual claim language, including all equivalents.

Respectfully submitted,

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